WEST BENGAL STATE UNIVERSITY

B.Sc. Honours 3rd Semester Examination, 2021-22

PHSACOR07T-PHYSICS (CC7)

Time Allotted: 2 Hours | Full Marks: 40

The figures in the margin indicate full marks.
Candidates should answer in their own words and adhere to the word limits as practicable.
All symbols are of usual significance.

Question No. 1 is compulsory and answer any *two* from the rest

1. Answer any ***ten*** questions from the following: 2×10 = 20

   (a) What is Monolithic IC? Write about its Fabrication.

   (b) What type of screen is used in CRT and why?

   (c) Magnetic deflection is desirable in CRTs for television: Explain why.

   (d) Write down the Boolean function corresponding to the following standard POS notation

   $$f(A, B, C) = \prod M(2, 3, 4, 7)$$

   (e) What is the difference between synchronous and asynchronous counters?

   (f) Draw the logic block diagram for adding two decimal numbers 7 and 12.

   (g) What is duty of cycle?

   (h) What is Veitch diagram?

   (i) A 4-bit D/A converter produces an output of 4.5 V for an input code of 1001. Find the output for an input code of 0011.

   (j) Difference between Ring counter and Decade counter. Add BCD numbers 0111 and 0101.

   (k) What is JK flip-flop? How many bytes are there in a 32-bit data word?

   (l) What is synchronous orbit?

   (m) The input to a logic gate are A = 1100 and B = 1010. What will be the logic gate if the output is 0110?

   (n) Show the logic symbol of full subtractor using half subtractor.

   (o) Show the pinout diagram of serial in and parallel out shift Register.

2. (a) Minimize the following function by using Karnaugh mapping technique and realize the resulting logic circuits by using minimum number of logic gates. 3+2

   $$f(A, B, C, D) = \sum m(0, 1, 2, 3, 11, 12, 14, 15)$$

(b) Introduce 2's complement method in binary subtraction process. Hence draw a 4-bit binary adder/subtractor circuit and briefly explain its operation. 1+2+2

3. (a) Write the truth table of Half Subtractor and draw its logic diagram. 2+2

(b) What advantage does a J-K flip-flop have over an SR flip-flop? Why the restriction of pulse width is necessary in JK flip-flop? 1+1

(c) An 12 MHz square wave clocks a 6-bit ripple counter. What is the frequency of the last flip-flop? 2

(d) How any flip-flop is required for Mod-17 counter? What is BCD counter? 1+1

4. (a) Add 54 with –22 using 2's complement method. 3

(b) Draw the logic diagram of a 4-bit ring counter. 2

(c) What do you mean by resetting of a counter? How many state do a 5-bit ripple counter have? 1+1

(d) What is a single bit Register? What is known as universal shift register? 1+2

5. (a) A sine wave is displayed on CRO screen with the calibrated time base set at 0.1 ms/div. One cycle of displayed waveform spreads over 10 divisions along the horizontal axis. Find the frequency of the waveform. 2

(b) How is a J-K flip-flop made to toggle? 2

(c) Master-slave J-K flip-flops are called pulse-triggered or level-triggered devices. — Why? 3

(d) Draw a 4-bit serial-in, serial-out shift register using J-K flip-flops and show output stages. 3

N.B. : *Students have to complete submission of their Answer Scripts through E-mail / Whatsapp to their own respective colleges on the same day / date of examination within* 1 *hour after end of exam. University / College authorities will not be held responsible for wrong submission (at in proper address). Students are strongly advised not to submit multiple copies of the same answer script.*

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